SQUID MODULE V1 (3U) TEST PROCEDURE

Created: 9/9/98
Revised: 9/28/98
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File Location: CO-OP PC (PPD 1075)\\ E:\Cdms\Squid\squid_test_proc.doc

This document should be used along with the "Squid Users Manual" to test and/or troubleshoot the 3U Squid Module.

I. INTRODUCTION:

This test procedure is for a Squid V1 board and is intended to help test and/or troubleshoot a Squid V1 Module. A Squid board that is being built and tested should be able to pass this test and meet all other specifications given to it before it can officially be "stamped" as a Squid V1 module. Similarly, all Squid boards sent back for repair should once again pass this test before they are sent out for operation again.

This procedure is written for testing in the 10th floor lab in Wilson Hall at Fermilab.

II. TEST EQUIPMENT REQUIRED:

1. GPIB Interface
2. 3U Controller Card Version "D". Board # ISR-D.x
3. 3U Subrack, #3U-1.x
4. 3U Extender Card for subrack, #XB3-1.x
5. CDMS Power Supply, #PS-1.x
6. Tektronix 2467B 400MHz Oscilloscope
7. HP 33120A 15 MHz Function/Arbitrary Waveform Generator
8. HP 8012B Pulse generator.
9. Attenuater Box
10. 2 Co-axial Clip Leads
11. Unix Computer with **rack.pl –i squid.rack** software., loaded as follows:
    a) From any computer, telnet to **fnpx19**.
    b) Logon: **cdmsuser**
    c) Password: **#kryostat**
    d) Then **cd perl**.
    e) Type **rack.pl –i squid.rack**
    f) Command line should look like this: squid r2, m5

III. TEST PROCEDURE:

TEST SETUP:

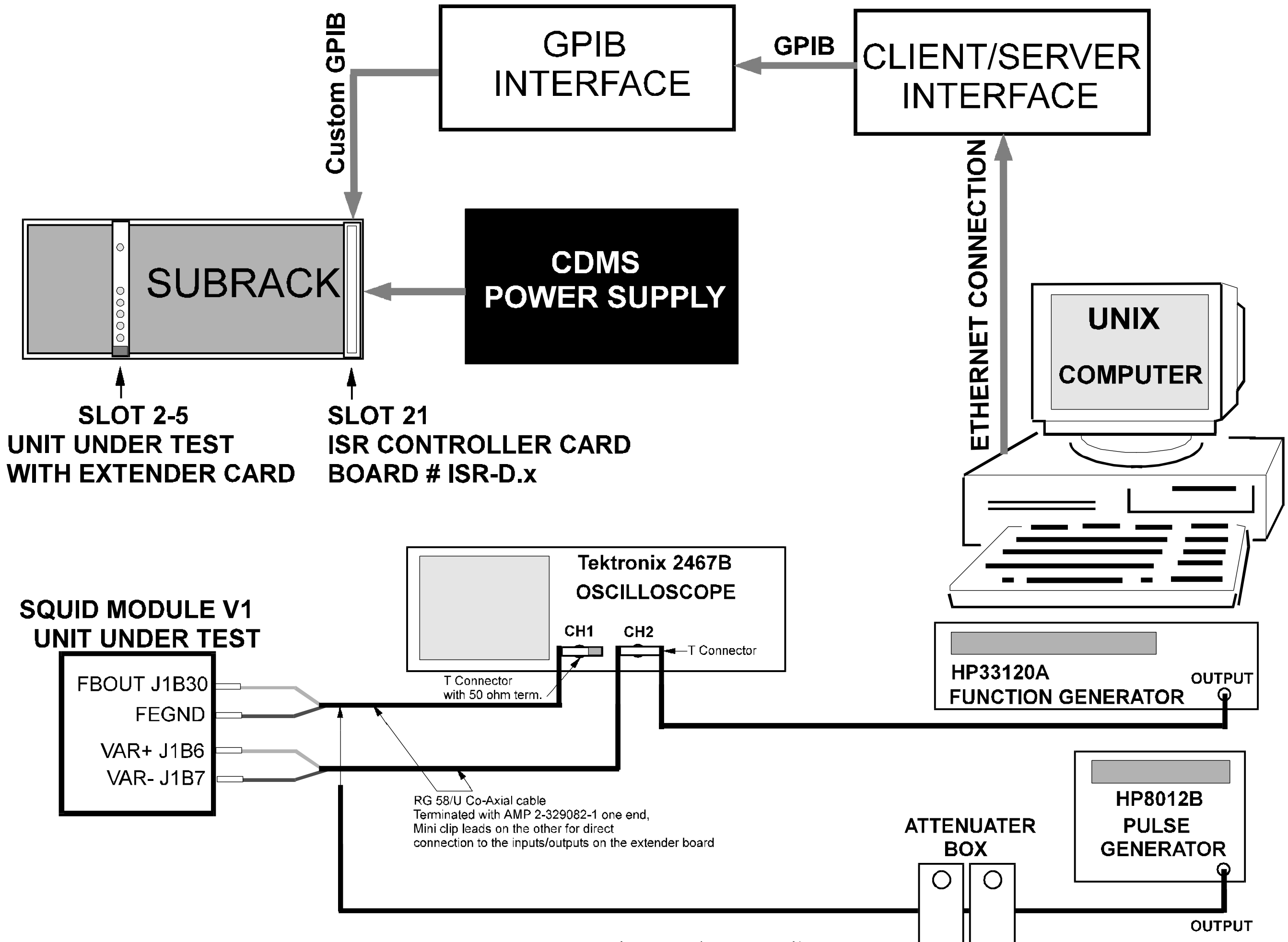

Figure 1: Test Setup

1) **Insert the Squid V1 module to be tested into one of the slots 2-5 with an extender card. Make sure to read each step thoroughly before testing each section.**

2) **Power section testing:**

a) Power up while watching the front panel LED display.
b) The +/-15V FE and A should come on after about 1.3 seconds.
c) After an additional .25 seconds, the +5 Digital LED should turn on.
d) Next, check the following voltage levels with the scope (or DMM) at the corresponding pins:

IC	PIN	VOLTAGE LEVEL	TOLERANCE
39	6	+15 A	+/- .25 V
Q5	2	-15 A	+/- .25 V
40	6	+ 15 FE	+/- .25 V
Q7	2	- 15 FE	+/- .25 V
1	3	+ 5 REF	+/- .02 V
1	14	-5 REF	+/- .02 V
23	1	+10 R	+/- .02 V

24	1	-10 R	+/- .02 V

e) Now check the noise on all power supplies by changing the scope to AC coupling and monitoring the voltage ripple levels on all of the supplies in step (d). The ripple should be below 10 mVpp on each supply.

3) Digital control/ module addressing section testing:

a) Next set the 4 pole blue DIP switch to match the slot number the board is being tested in. For example, if the unit under test is placed in slot 5, then the switch should be set as follows in **Figure 2** below. If the unit under test were in slot number 3 then the settings would be like the ones shown in **Figure 3**.

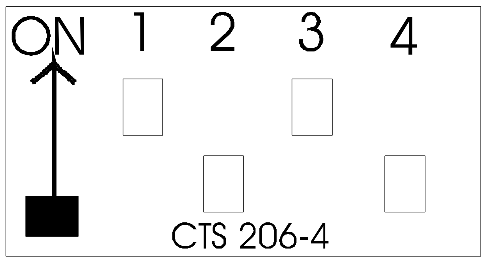

FIGURE 2
(SLOT 5 SWITCH SETTINGS)

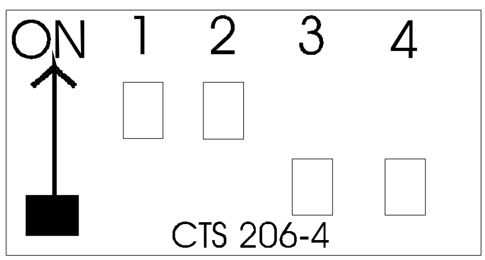

FIGURE 3
(SLOT 3 SWITCH SETTINGS)

b) Using the software command “**readSQUID(a)**”, check to see if the yellow “MOD ADD” LED on the front panel flashes multiple times each time this command is issued.

4) DAC Section testing:

a) Issue the following command, “**setSQUIDbias(5)**”, and test the DAC output for the Squid_Bias/V voltage at IC 2 pin 3, as specified in **Table 1**. (NOTE: the voltage is enclosed in parentheses within the command). This first command above was for a DAC setting of 5 volts. Next issue the command “**setSQUIDbias(-5)**”, and test Squid_Bias/V for the proper voltage level of –5 volts. Continue this same process with the remaining voltage levels below in **Table 1** for the “**setSQUIDbias(voltage)**” command. Repeat the above process to test the

Gain and FB_Offset (located in the output stage of the amplifier), using the following commands: “**setSQUIDolgain(voltage)**” for the Gain, and “**setLockPoint(voltage)**” for the FB_Offset The Offset_ADJ however, (located in the input stage of the amplifier), multiplies the input voltage by 10, so the voltage range entered via the software is +/**- 500** mV, instead of +/**- 5** V in the other two cases. Use the command “**setAmpOffset(voltage)**” to set this offset, making sure the entered voltages are between + and **- .5** V.

TEST	IC	PIN	VOLTAGE LEVEL	TOLERANCE
Squid_Bias/V	2	3	+5	+/- .1 V
			-5	
			+2	
			-2	
			0	
Gain	2	2	+5	+/- .1 V
			-5	
			+2	
			-2	
			0	
FB_Offset	2	27	+5	+/- .1 V
			-5	
			+2	
			-2	
			0	
Offset_ADJ	2	26	+5	+/- .1 V
			-5	
			+2	
			-2	
			0	

Table 1

5) Calibrate mode testing:

a) Using the software command “**openfb**”, place the UUT into “Calibrate” mode.
b) Check to see if this worked by looking for +5 volts on IC 12 pin 3, and 0 volts on pin 4.
c) Setup the function generator for a 2 Vpp, 10 Hz Sine wave.
d) Connect the “+” input to J1-B6 and the “–“input to J1-B7, as shown in **Figure 1**.
e) Monitor J1-B30 with the scope (relative to FEGND), using the clip leads and terminating the scope input with 50 ohms. Trigger the scope on the input signal on channel 2, as shown in **Figure 1**. This signal should either be in phase or inverted relative to the input signal, depending on the state of the relay before the previous power down/power up cycle. The amplitude should be about 540 mVpp.
f) Using the software commands “**polposSQUID**” and “**polnegSQUID**”, toggle the polarity and make sure the output toggles between inverted and in phase relative to the input respectively. Before continuing, set the polarity back to positive with the software command “**polposSQUID**”.
g) Remove the variable signal coming from the function generator and input at J1-B27 (again relative to FEGND,) a pulse coming from the attenuater box. The input to the attenuater box should come from the pulse generator, (setup shown in **Figure 1**,) with 1 V amplitude, 5 usec pulse width, and 1 msec period. Attenuate this pulse by 30 dB, and verify that the amplitude after attenuation is about 33 mV.
h) Monitor IC 3 pin 6 with the scope probe, again triggering on the input signal. This signal should be in phase and have an amplitude of 540 mV. If there is a DC offset, adjust it to 0 volts using the “**setAmpOffset(voltage)**” command.
i) Monitor IC 4 pin 6 with the scope probe, (relative to FEGND). This signal should be an inverted version of the signal observed in step “h”. The gain is dependent on the DAC voltage set with the software command “**setSQUIDolgain(voltage)**”. Set this voltage to

whatever it takes to make this signal have an amplitude of about –1V. (Should be somewhere in the range of 1 to 1.5 volts).

j) Monitor J1-B2 with the scope, (relative to FEGND), again using the clip leads and terminating the scope input with 50 ohms. This signal should be an inverted version of the signal in step "i" (in phase with the input). If there is a DC offset, adjust it to 0V using the opposing DAC voltage set with the command "**setLockPoint(voltage)**".

k) If this all works, the "Calibrate" mode works.

6) Measure mode testing:

a) Using the software command "**closefb**", place the UUT into "Measure" mode.

b) Check to see if this worked by looking for 0V on IC 12 pin 3, and +5V on pin 4.

c) Input at J1-B27 (relative to FEGND), a pulse coming from the attenuater box. The input to the attenuater box should come from the pulse generator, (setup shown in **Figure 1**), with 1 V amplitude, 5 usec pulse width, and 1 msec period. Attenuate this pulse by 30 dB, and verify that the amplitude after attenuation is about 33 mV.

d) Monitor IC 4 pin 6 with the scope probe, (relative to FEGND). This signal should be an inverted version of the input signal. The gain is dependent on the DAC voltage set with the software command "**setSQUIDolgain(voltage)**". Set this voltage to whatever it takes to make this signal have an amplitude of about –1V. (Should be somewhere in the range of 1 to 1.5 volts).

e) Monitor IC 7 pin 7 with the scope. This should be an integrated version of the signal from step "d". The fall time should be approximately 70 usec, the rise time 5 usec, and the amplitude about 1.5 V, which is dependent on the voltage level of the DAC set in step "d".

f) Monitor J1-B30 with the scope (relative to FEGND), using the clip leads and terminating the scope input with 50 ohms. This signal should be an inverted version of the signal in step "e".

g) Monitor J1-B2 with the scope (relative to FEGND), using the clip leads, but this time NOT TERMINATING the scope input. This signal should be in phase with the signal from step "f" (out of phase with the input), with an amplitude of about 1.5 V. If there is a DC offset, adjust it to 0V using the opposing DAC voltage set with the command "**setLockPoint(voltage)**". If the integrator is clipped, reduce the open loop gain, originally set in step "d".

h) If this all works, the "Measure" mode works.

7) ZAP Circuit testing:

a) Enable the "ZAP" circuitry with the front panel switch.

b) Using the software command "**ASynchZapMode**", place the UUT into the "Asynchronous" mode.

c) Using the software command "**ZapVolt(voltage)**", set the "Zap Voltage" to one of four possible values: **0, 1.25, 2.5, or 3.75**. Use **3.75** volts to start with for now.

d) Using the software command "**ZapWidth(pulse width)**", set the pulse width of the "Zap Signal" to one of sixteen possible values: **100, 200, 300, … 1600** msec**.** Use **100** msec. for the first test.

e) Monitor J1-B27 with the scope (relative to FEGND) using the clip leads, but this time NOT TERMINATING the scope input. "ZAP" the circuit using the software command "**armZapSQUID**". This should produce a 3.75 volt pulse with a width of 100 msec.

f) Repeat steps "d" and "e" for the remaining widths at a voltage of 3.75 volts.

g) Next change the voltage to **2.5** volts using the command in step "c", but leave the width at **1600** msec. Zap the circuit while monitoring J1-B27. The pulse should have an amplitude of 2.75 volts with a width of 1600 msec. Repeat this process with a voltage of **1.25** and **0** volts.

h) Using the software command "**SynchZapMode**", place the UUT into the "Synchronous" mode.

i) Using the software command “**ZapVolt(voltage)**”, set the “Zap Voltage” to **3.75** volts.

j) Using the software command “**ZapWidth(pulse width)**”, set the pulse width of the “Zap Signal” to **1600** msec**.**

k) Again monitor J1-B27 with the scope while ATTEMPTING to “ZAP” the circuit using the software command "**armZapSQUID**”. This should NOT produce a pulse of voltage and width corresponding to the settings from steps “i” and “j”.

l) Now trigger the ZAP circuit using a pulse of 300 mV in amplitude, 5 usec pulse width. The “+” input should be on J1-B3, and the “**-**“ input on J1-B4.

m) Immediately after this trigger signal is applied, the circuit should “ZAP”. Verify this by observing the output at J1-B27 with the scope. This output should be 3.75 V in amplitude, with a width of 1600 msec.

n) If this all works, the “ZAP” circuitry works.